REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

The Applicants noticed that certain references in the filed Information Disclosure Statements (IDS) are lined-through and have not been considered. Consideration of is respectfully requested, for the reasons explained below. First, five foreign references, copies of which were provided, in the IDS filed 10/26/04 are lined through. See the attachment to the 3/02/07 Office Action. These references are listed in the International Search Report (ISR) filed with the IDS, which indicates the categories (such as X and Y) for each of the five references. According to MPEP §609.04(a), the search report categories satisfies the requirement for the statement of relevancy. All requirements are met and these references should be considered. Consideration is respectfully requested.

The Applicants filed an IDS on 12/07/07 citing several references from three related Japanese Office Actions.[1] All of the foreign references were lined through. According to MPEP §609.04(a), a translation of the foreign office action which indicates the degree of relevance found by the Japanese Patent Office satisfies the requirement of a statement of relevancy. The relevance of JP 2001-210122 and WO/91095 is discussed in the office actions. It is respectfully submitted that all requirements are met for these references, and they should be considered. The remaining references (JP 2003-150118, JP 2003-150109 and JP 2003-216100) were considered relevant enough to be cited in the office actions. Consideration of these three references is also respectfully requested.

The drawings were objected to under 37 C.F.R. § 1.83(a) in paragraphs 3 and 4 of the Office Action. The Applicants also appreciate the discussion with Examiner Chowdhury regarding proposed changes to the drawings. The Applicants proposed to amend Figures 67 and 178 to show a frame period. Examiner Chowdhury suggested to submit amended

[1] A corrected PTO-1449 form was submitted on January 3, 2008.

drawings illustrating a frame period, and she would consider whether the objections should be withdrawn. The Applicants have submitted new Figures 67 and 178 to address the objections made in paragraph 4 of the Office Action. The figures are amended to indicate the frame period for the horizontal scanning periods. Approval of the new drawings 67 and 178 is respectfully requested.

Regarding the objections to the drawings in paragraph 3 of the Office Action, the claims are amended and the support for the amended claims is explained below. It is respectfully submitted that the drawings support the amended claims and withdrawal of the objection noted in paragraph 3 of the Office Action is respectfully requested.

Claims 1-8 and 10-21 are present in this application, claim 9 being cancelled and claims 16-21 being added by way of the present amendment. Under 35 U.S.C. § 103(a), claim 3 is rejected over U.S. 6,765,549 (Yamazaki et al.) and claims 1, 2, 4-7, 9, 10 and 15 are rejected over Yamazaki et al. in view of U.S. 6,583,775 (Sekiya et al.). Claims 8 and 11-14 are withdrawn from consideration.

Amended claim 1 is supported in general, for example, by the non-limiting disclosure of Figure 1 and page 72, line 22-page 73, line 3 and page 77, lines 9-12. Amended claim 1 recites a gate driver circuit that generates a plurality of stripe non-display areas on a display screen of the EL display by controlling the first switching elements, and moves the plurality of stripe non-display areas in a scanning direction of the gate driver circuit. An operation for retaining an image signal applied to each pixel is executed only once during the frame period. The Applicants refer the Examiner to the non-limiting example of Figure 16 and page 60, lines 16-22, and to Figures 19(b)-19(c) and page 176, lines 11-24. Gate driver circuit 12 moves the plurality of stripe non-display areas 52 on the display screen in the scanning direction of the driver circuit 12.

Claim 1 is also supported, for example, by the non-limiting disclosure of Figure 17(a) and page 163, lines 3-11 with regard to the recited operation. In this non-limiting example, gate signal line 17a applies an ON signal (Vgl) to transistor 11c in one period of 1H during which one pixel row is selected and then the image signal is written into each pixel 16.

Claim 2 recites a gate driver circuit which selects a pixel row of the EL display in sequence, wherein a start pulse to be input into the gate driver circuit is controlled. A plurality of stripe non-display areas on a display screen of the EL display are generated and the plurality of stripe non-display areas are moved in a scanning direction of the gate driver circuit. The gate driver circuit is supported, for example, by the non-limiting disclosure at page 160, lines 16-22 and Figure 16. The start pulse input to the gate driver circuit is supported by the non-limiting example of page 88, lines 8-22, for example. The plurality of stripe non-display areas is supported by, for example, the non-limiting disclosure of page 218, line 25 – page 219, line 2. Reference is also made to page 174, line 13 – page 175, line 6, as further non-limiting support.

Claim 5 is amended to recite that each of the second switching elements has a plurality of transistor elements, each of the first switching elements and each of the second switching elements are constituted so that the first and second switching elements are controlled independently of each other for turning on and off by the first and second gate driver circuits, and the first gate driver circuit generates stripe non-display areas on a display screen of the EL display panel and moves the plurality of stripe non-display areas in a scanning direction of the gate driver circuit. Claim 5 is supported, for example, by the non-limiting disclosure of Figures 1 and 42, and page 72, line 22 – page 73, line 3. See driver circuits 12a and 12b and transistors 11c and 11d, for example. Claim 5 is also supported by the non-limiting disclosure on page 266, lines 4-13.

New claims 16, 17, 20 and 21 are supported by, for example, the non-limiting disclosure on page 56, line 20 – page 57, line 2 and new claims 18 and 19 are supported by, for example, the non-limiting disclosure on page 174, lines 1-12.

Accordingly, no question of introduction of new matter is believed to be raised by the amended or new claims.

The claims of the present application are directed to a drive method for an EL display panel and an EL display panel. In the drive method, a plurality of stripe non-display areas on a display screen are generated and the plurality of stripe non-display areas are moved in a scanning direction of the gate driver circuit. With such features, the frame rate of an image display can be lowered, resulting in reduced power consumption and flickering, as described in the non-limiting disclosure in the last paragraph on page 162. Further, by varying the proportion of the plurality of non-stripe display areas in the entire display screen, it is possible to control the display brightness of the screen.

Turning to the prior art rejections, Yamazaki et al. describe a drive system for a pulse width modulation method. Yamazaki et al. teaches that image data is written for each line of pixel row by applying the prescribed pulse. However, this reference does not disclose or suggest the methods of claims 1 and 2 where a plurality of stripe non-display areas are displayed on a display screen of the EL display panel and a plurality of stripe non-display areas are moved in a scanning direction by a gate driver circuit.

Sekiya et al. teaches that an image is displayed in the first half of one frame, and in the later half of the frame the image is extinguishes as if the brightness of the CRT were attenuated, as explained in column 16, line 66 – column 17, line 28. However, Sekiya et al. likewise fails to disclose or suggest the methods of claims 1 and 2 having a plurality of stripe non-display areas displayed on a display screen of an EL panel and a plurality of stripe non-display areas are moved in a scanning direction of the gate driver circuit. Withdrawal of the

rejection of claims 1 and 2 based upon Yamazaki et al. considered alone or with Sekiya et al. is respectfully requested.

Claim 5 recites that each of the switching elements has a plurality of transistor elements and the first gate driver circuit generates stripe non-display areas on the display screen of the EL display panel and moves the plurality of stripe non-display areas in a scanning direction of the first gate driver circuit. As described above, neither Yamazaki et al. nor Sekiya et al. disclose or suggest such a gate driver circuit. Accordingly, claim 5 is also patentably distinguishable over Yamazaki et al. considered alone or with Sekiya et al.

Claim 15 recites a display apparatus having the display panel according to claim 5 and a receiver. Claim 15 is patentable over the applied prior art for the same reasons discussed above for claim 5.

It is respectfully submitted that the present application is in condition for allowance, and a favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Registration No. 28,870

Carl E. Schlier
Registration No. 34,426

Attorneys of Record

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/07)